IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claim 1, in accordance with the following:

1. (CURRENTLY AMENDED) A reset control system of a system having a central processing section and a peripheral control section which are formed on separate chips, said reset control system comprising:

an emulator; and

a system reset output section generating and outputting a system reset signal on the basis of an external reset signal and an emulator reset signal based on a reset instruction from the emulator to independently implement a function of said central processing section,

wherein said system reset signal output from said system reset output section is supplied to both chips of said central processing section and said peripheral control section.

2. (PREVIOUSLY PRESENTED) The reset control system according to claim 1, wherein said system reset signal is generated by OR-operating said emulator reset signal and said external reset signal.

3. (PREVIOUSLY PRESENTED) The reset control system according to claim 1, wherein said system reset output section is provided in the chip of said peripheral control section.

4. (PREVIOUSLY PRESENTED) The reset control system according to claim 1, wherein said system reset output section is provided in the chip of said central processing section.

5. (PREVIOUSLY PRESENTED) The reset control system according to claim 1, further comprising:

a mask processing section masking said external reset signal when said emulator is in operation.

6. (PREVIOUSLY PRESENTED) The reset control system according to claim 1, further comprising:

a synchronization processing section synchronizing activation timings after reset between said central processing section and said peripheral control section, said synchronization processing section being formed on at least one of the chips of said central processing section and said peripheral control section.

7. (PREVIOUSLY PRESENTED) The reset control system according to claim 6, wherein said synchronization processing section comprises an activation enable signal output section for outputting an activation enable signal for instructing to enable activation after elapse of a predetermined time after reset of said central processing section or said peripheral control section.

8. (PREVIOUSLY PRESENTED) The reset control system according to claim 5, further comprising:

a synchronization processing section synchronizing activation timings after reset between said central processing section and said peripheral control section, said synchronization processing section being formed on at least one of the chips of said central processing section and said peripheral control section.

9. (PREVIOUSLY PRESENTED) The reset control system according to claim 8, wherein said synchronization processing section comprises an activation enable signal output section for outputting an activation enable signal for instructing to enable activation after elapse of a predetermined time after reset of said central processing section or said peripheral control section.

10. (PREVIOUSLY PRESENTED) A reset control system of a system having a central processing section and a peripheral control section which are formed on separate chips, said reset control system comprising:

an emulator;

a reset selection section selectively outputting, as a system reset signal, one of an external reset signal and an emulator reset signal based on a reset instruction from the emulator to independently implement a function of said central processing section,

wherein said system reset signal output from said reset selection section is supplied to both chips of said central processing section and said peripheral control section.

11. (PREVIOUSLY PRESENTED) The reset control system according to claim 10, further comprising:

a synchronization processing section synchronizing activation timings after reset between said central processing section and said peripheral control section, wherein said synchronization processing section is formed on at least one of the chips of said central processing section and said peripheral control section.

12. (PREVIOUSLY PRESENTED) The reset control system according to claim 11, wherein said synchronization processing section comprises an activation enable signal output section for outputting an activation enable signal for instructing to enable activation after elapse of a predetermined time after reset of said central processing section or said peripheral control section.

13. CANCELLED

14. (PREVIOUSLY PRESENTED) A reset control method of a system having a central processing section and a peripheral control section which are formed on separate chips, said method comprising:

masking an external reset signal when an emulator that independently implements a function of said central processing section is in operation;

generating a system reset signal on the basis of the masked external reset signal and an emulator reset signal based on a reset instruction from said emulator; and

supplying said system reset signal to both chips of said central processing section and said peripheral control section.

15. (PREVIOUSLY PRESENTED) The method according to claim 14, wherein said system reset signal is generated by OR-operating said emulator reset signal and said masked external reset signal.

16. (PREVIOUSLY PRESENTED) A reset control method of a system having a central processing section and a peripheral control section which are formed on separate chips,

said method comprising:

selectively outputting, as a system reset signal, one of an external reset signal and an emulator reset signal based on a reset instruction from an emulator to independently implement a function of said central processing section; and

supplying said system reset signal to both chips of said central processing section and said peripheral control section.